Notice of Allowability	Application No.	Applicant(s)	
	09/672,424	SAUND ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment and declaration filed10/16/06*.

2. ☒ The allowed claim(s) is/are *1,3-6,8-9,12-58*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Eric Coleman
Primary Examiner

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance: The combination of claimed features in the independent claims was not found in the prior art. The combination in claim 1 comprises detecting that an iteration completes operation of the macroinstruction, adding a marker indicating the end of the macroinstruction to a microinstruction in the pipeline downstream of the decoder; after reaching a termination condition of the macroinstruction, partially executing an iteration beyond the termination , the partial execution committing at least one side effect to an architecturally visible resource of the computer, and raising an exception to transfer control to a second microinstruction stream . These features in combination with the other limitations in claim 1 was not found in the prior art. Also the variation to this combination of features in claim 23 was not found in the prior art. The variation to this combination of features in claim 55 also was not found in the prior art.

The combination of features in claim 5 comprises decoding a macroinstruction of a computer, the decoding of the macroinstruction generating a plurality of iterations of: a pattern of microinstructions implementing a basic operation, wherein the microinstruction set architecturally exposed to programs fetched from an architecturally-visible memory of the computer and a branch instruction predicted not taken. This combination of features was not found in the prior art.

The combination of features in claim 13 comprises the decoding of the internal-iteration macroinstruction designed to generate a plurality of iterations of: a pattern of macroinstructions for implementing a basic operation of an internal iteration of the

internal-iteration macroinstruction , and a branch microinstruction predicted not taken, wherein the branch microinstruction is to be generated carrying a marker indicating that the branch microinstruction defines a boundary between two successive iterations of the internal-iteration microinstruction. These features in combination with the other limitations in claim 13 was not found in the prior art.

The combination of features in claim 14 comprises decoding a macroinstruction on a computer the macroinstruction calling for a plurality of iterations of a sequence of one or more microinstructions; and on detecting that an iteration completes operation of the macroinstruction, adding a marker indicating the end of the macroinstruction to a microinstruction in the pipeline downstream of the decoder. This combination of features was not found in the prior art.

The combination in claim 20 comprises a computer comprising: an instruction decoder designed to decode a macroinstruction set that includes a macroinstruction calling a plurality of iterations of a sequence of one or more microinstructions; a pipeline stage downstream of the instruction decoder designed to detect that operation of the macroinstruction is complete, and in response, to add to a microinstruction a marker indicating the end of the macroinstruction. This combination of features was not found in the prior art.

The combination in claim 30 comprises a computer comprising: circuitry designed to partially execute a post termination iteration of a loop of a first microinstruction stream executing in the computer, the partial execution designed to commit at least one side effect to an architecturally-visible resource of the computer,

and to raise an exception to transfer control to a second microinstruction stream; software of the second microinstruction stream, programmed to unwind side-effects committed by the post termination iteration. This combination of features was not found in the prior art.

The combination in claim 35 comprises in a computer having instruction fetch circuitry for fetching instructions in first and second instruction sets from a memory of the computer and executing the instructions, executing a first instruction coded in the first instruction set, the first instruction storing into a memory location a value of a second instruction coded in the second instruction set, in response to the storing, clearing an instruction cache and execution pipeline of the computer of the former content of the memory location; executing the second instruction in the execution pipeline. This combination of features was not found in the prior art. The variation to this combination of features in claim 41 also was not found in the prior art.

The prior art comprises allowing a pipeline to drain (i.e., emptying the pipeline gradually or completely) such as when as the time when a pipeline processes all the instructions of a thread. The combination of features in claim 44 comprises decoding and executing an instruction on a computer, execution of the instruction comprising the steps of waiting to allow a pipeline to drain, and setting, bits of a floating-point control word to values denoted in an explicit immediate field of the instruction. This combination of features was not found in the prior art. Claim 49, comprises a computer comprising: execution circuitry designed to execute an instruction calling for waiting a pipeline to drain and set bits of a floating point-control word to values denoted in an

explicit immediate field of the instruction. This combination of features was also not found in the prior art.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ERIC COLEMAN
PRIMARY EXAMINER